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EXAMINER
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THOMAS, MIA M

ART UNIT	PAPER NUMBER
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2609 <sup>RP</sup>

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05/18/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/823,374

**Applicant(s)**

VERBECK ET AL.

**Examiner**

Mia M. Thomas

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☒ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date see attached.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 1,10,11,15 and 17 are objected to because of the following informalities: Line 1 of Claim 1 recites: "a method of implementing a discrete cosine transform (DCT) in a graphics processing unit (GPU)." The uses of parenthesis in this instance are objected to for the following reasons. First, the use of parenthesis in a sentence is typically limited to the inclusion of unimportant, or superfluous information and unimportant, or superfluous information should not be recited in a patent claim with one exception. The MPEP, at paragraph 608.01(m) allows for the enclosure of reference numerals, corresponding to the figures, within parenthesis. However, in this case, the term(s) "discrete cosine transform" and "graphics processing unit" are not reference numerals. It is suggested that applicant choose the most appropriate terms for inclusion in the claim, and delete the other. For example, applicant should use DCT or discrete cosine transform and GPU or graphics processing unit in all dependent claims respectively. Appropriate correction is required.

### ***Claim Objections - 37 CFR 1.75(a)***

2. The following is a quotation of 37 CFR 1.75(a):

The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery.

Claims 2 and 14 are objected to under 37 CFR 1.75(a), as failing to conform to particularly point out and distinctly claim the subject matter which application regards as his invention or discovery.

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**Regarding Claim 2**, the method of claim 1, wherein the multiplying, determining and sampling are performed by the GPU. The term “the multiplying is unclear as to which multiplying the applicant is exactly claiming with reference to the invention. The phrase multiplying, for example, is used twice with regards to independent claim 1. Claim suggestions include:

... wherein the multiplying of a column or row of pixels with a predetermined matrix to generate a corresponding set of output pixels and determining and sampling of the pixels are performed by the GPU.

**Regarding claim 14**, the method of claim 13, wherein setting up the shaders and rendering are performed in the GPU. The terms “rendering” and “the shaders” are not supported with respect to independent claim 13. The term should clearly state what the applicant intends to “render”. Claim suggestions include:

...wherein setting up the shaders and the rendering are performed in the GPU.

Appropriate correction is required.

**Regarding claim 14**, the term GPU at claim 14, line 2 lacks an antecedent basis.

However, it appears from the context of the claim when read in light of the specification that the “GPU” is in fact referring to the graphics processing unit first introduced at line 1 of claim 1; and this will be assumed for examination purposes. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. **Regarding Claim 15**, a system to program a graphics processing unit (GPU) to implement a discrete cosine transform (DCT); the claim has a preamble with no structure. *The [a] system* as claimed should be represented by the applicant's claimed subject matter. Claim suggestions include:

A system comprising: a graphics processing unit (GPU) to implement a DCT and a device adapted to program said GPU.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Chow et al. (US 6, 292,589 B1).

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**Regarding Claim 1**, Chow discloses a method of implementing a discrete cosine transform (DCT) in a graphics-processing unit (GPU) ("At step 442, a Discrete Cosine Transform (DCT) is applied to the block of pixels to provide image enhancement, restoration, and facilitate encoding of the image." at column 26, line 22; "FIG. 2 is a block diagram of a computer system incorporating the present invention" at column 3, line 28 which incorporates a graphics controller (Figure 2, numeral 26); comprising: separating an image into blocks of pixels (Refer to Figure 5b; "The method includes compressing, using the assigned quantization values, a macroblock such that a resultant compressed macroblock is represented by a subset of bits used to represent said macroblock." at column 3, line 4); for each block of pixels, in parallel, multiplying a column or row of pixels with a predetermined matrix to generate a corresponding set of output pixels ("Similarly, the order of operations is important to developing the optimal solution...by allowing IDCT and DCT to be executed in parallel." at column 45, line 36), "Referring now to FIG. 31A, the above described approach to DCT and IDCT computing can be provided via the DCT Unit data path implementation 674, which is shown to include 4 functional units. The fourth unit is a multiplier unit 678." at column 45, line 41); determining sets of scan-lines based on the sets of output pixels ("The spider diagram may be read left to right and by interpreting constants above a horizontal scaling line (k1-k10) as scaling factors, and where two lines meet at a vertex a summation occurs." at column 45, line 23) and for each set of scan-lines, sampling at least a portion of the pixels comprised within the scan-lines and pixels relative to the scan-lines, and multiplying the sampled pixels with a row or column of the predetermined matrix ("Here,

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the coefficients are stored using the specific ordering and location in structure 720 to support transformation of the 8 x 8 pixel array of FIG. 32." at column 47, line 36).

**Regarding Claim 2**, Chow discloses the method of claim 1, wherein the multiplying, determining, and sampling are performed in the GPU ("Referring now to FIG. 31A, the above described approach to DCT and IDCT computing can be provided via the DCT Unit data path implementation 674, which is shown to include 4 functional units. The first is the double buffer operand store 646. The second and third functional units are adders 676 and 677. Each adder has four associated scratchpad registers 675. These registers are 2 write/2 read port registers. Each adder is capable of performing 2's complement addition or subtraction. The fourth unit is a multiplier unit 678." at column 45, line 41).

**Regarding Claims 3 and 18**, Chow discloses the method and system wherein each corresponding set of output pixels corresponds to a textured line across the pixels in the blocks of pixels (Referring to Figure 19(b) and Figure 21, the macroblock templates to be inputted are considered at step 464 (Figure 21), bi directional which resolves that the output pixels will correspond to a textured line across the pixels).

**Regarding Claim 4**, Chow discloses the method of claim 1, wherein sampling the pixels comprised within the scanlines comprises using a separate shader for each set of scanlines (Referring to Figures 6(a)-6(c); "Referring briefly to FIGS. 6A and 6B, the motion estimation process will be described with reference to a series of frames 60. Each frame of the series 60 includes pixels designated via (x, y) coordinates..."As seen in FIG. 6B, motion estimation is shown to include 3 discrete steps; a block matching

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step 66, a motion vector generation step 67 and an energy calculation step 68. Block-matching techniques are used to identify macroblocks in the preceding (and/or succeeding) frames, which have the best match of pixel values to the macroblock of interest in the current frame. The macroblock matching procedure may be performed using a series of adder circuits or other methods apparent to those in the art." at column 10, line 18).

**Regarding Claims 5 and 20,** Chow discloses the method and a system further comprising wherein the GPU defines an array of coordinate offsets to neighboring pixels, wherein the shader accesses the pixels in the scanlines using the offset array ("Here, the coefficients are stored using the specific ordering and location in structure 720 to support transformation of the 8 x 8 pixel array of FIG. 32." at column 47, line 36).

**Regarding Claims 6 and 21,** Chow discloses the method and a system wherein the same shader can be used for each pixel in a scanline ("The DFU is responsible for reducing the amount of video data by means of sub-sampling and decimation of horizontal scan lines as they arrive by optionally keeping only half the scan lines, either even or odd." at column 7, line 28; The hardware or circuit used to perform the DCT transform must be made as fast and as simple as possible. It is highly desirable to use the same physical logic gate for as many parts of the transform as possible, since to do so results in the fewest number of transistors needed to perform the operation. The fewer the number of transistors used, the faster and more economical the circuit will be." at column 45, line 66).

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**Regarding Claim 7**, Chow discloses a method of processing pixels comprising:

separating an image into blocks of pixels (Refer to Figure 5b; "The method includes compressing, using the assigned quantization values, a macroblock such that a resultant compressed macroblock is represented by a subset of bits used to represent said macroblock." at column 3, line 4); creating a polyline of pixels for each column or row in each block of pixels and creating a line for each row or column in each block of pixels ("The 8x8 2-D DCT is performed by evaluating the eight 1-D row transforms, then evaluating these results through 8 column transforms." at column 45, line 20); wherein the rows or columns correspond to the polylines created for each column or row ("The spider diagram may be read left to right and by interpreting constants above a horizontal scaling line (k1-k10) as scaling factors, and where two lines meet at a vertex a summation occurs." at column 45, line 23).

**Regarding Claim 8**, Chow discloses the method of claim 7, further comprising:

creating a polyline of pixels for each row or column in each block of pixels ("The 8x8 2-D DCT is performed by evaluating the eight 1-D row transforms, then evaluating these results through 8 column transforms." at column 45, line 20); and creating a line for each column or row in each block of pixels, wherein the rows or columns correspond to the polylines created for each row or column (Refer to Figure 32; "FIG. 32 illustrates a partitioning of a block of video data into left and right halves for row transforms, and into top and bottom halves for column transforms, for purposes of the DCT operation of FIG. 31" at column 4, line 52).

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**Regarding Claim 9**, Chow discloses the method of claim 7, further comprising:

determining sets of scanlines based on the lines created for each row or column in each block of pixels; and for each set of scanlines, sampling the pixels comprised within the scanlines and multiplying the sampled pixels with a row or column of a predetermined matrix ("Here, the coefficients are stored using the specific ordering and location in structure 720 to support transformation of the 8 x 8 pixel array of FIG. 32." at column 47, line 36).

**Regarding Claim 10**, Chow discloses the method of claim 7, wherein the steps of creating are performed in a graphics processing unit (GPU) (Referring to Figure 28, numeral 20 (PCI Local Bus), the portion of Figure 28 allows the graphics controller (26) of Figure 2 to show that it is connected to the PCI Local bus).

**Regarding Claim 11**, Chow discloses a method of processing pixels, comprising: separating an image into blocks of pixels (Refer to Figure 5b; "The method includes compressing, using the assigned quantization values, a macroblock such that a resultant compressed macroblock is represented by a subset of bits used to represent said macroblock." at column 3, line 4); determining a polyline of pixels for each column or row in each block of pixels ("The 8x8 2-D DCT is performed by evaluating the eight 1-D row transforms, then evaluating these results through 8 column transforms." at column 45, line 20); for each pixel in the polyline, sampling at least a portion of the other pixels in the corresponding column or row that lies along the polyline and pixels relative to the column or row; multiplying each of the other pixels by a discrete cosine transform (DCT) coefficient from a predetermined matrix to generate resultant values;

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and adding the resultant values together to generate a resulting value (Referring to Figure 19(a) and 19(b); "Procedures available for the application of a DCT to the pixel block are well known to those of skill in the art. The preferred embodiment of the invention implements DCT using hardware capable of performing ...DCT..." at column 6, line 60; "Referring again to FIGS. 19A and 19B, the results of applying the DCT of Equation 9A on block 430 are shown in block 432. The block 432 comprises the remaining DC values of the pixels, after the transform." at column 27, line 3).

**Regarding Claim 12**, Chow discloses the method of claim 11, further comprising biasing and scaling at least one of the polyline of pixels, the resultant values, and each resulting value for each pixel ("Prior to writing the row or column results into the double buffer 646, each result must be rounded via an incrementer 681, which is a non-biased two's complement rounding unit." at column 45, line 51).

**Regarding Claim 13**, Chow discloses a method of processing pixels, comprising: separating an image into blocks of pixels ("(Refer to Figure 5b; "The method includes compressing, using the assigned quantization values, a macroblock such that a resultant compressed macroblock is represented by a subset of bits used to represent said macroblock." at column 3, line 4)); for each column in a block of pixels setting up a shader and rendering a scanline; and for each row in a block of pixels, setting up a shader and rendering a column (Referring to Figures 6(a)-6(c); "Referring briefly to FIGS. 6A and 6B, the motion estimation process will be described with reference to a series of frames 60. Each frame of the series 60 includes pixels designated via (x, y) coordinates..."As seen in FIG. 6B, motion estimation is shown to include 3 discrete

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steps; a block matching step 66, a motion vector generation step 67 and an energy calculation step 68. Block-matching techniques are used to identify macroblocks in the preceding (and/or succeeding) frames, which have the best match of pixel values to the macroblock of interest in the current frame. The macroblock matching procedure may be performed using a series of adder circuits or other methods apparent to those in the art." at column 10, line 18).

**Regarding Claim 14**, Chow discloses the method of claim 13, wherein setting up the shaders and rendering are performed in the GPU (Referring now to FIG. 2, a computer system 10 for use with the present invention is shown to include a central processing unit (CPU) 12...Also coupled to the PCI bus is a graphics controller 26..." at column 5, line 44).

**Regarding Claim 15**, Chow discloses a system comprising: a graphics processing unit (GPU) to implement a DCT and a device adapted to program said GPU (Referring to Figure 2, numeral 26 (Graphics controller) and "At step 442, a Discrete Cosine Transform (DCT) is applied to the block of pixels to provide image enhancement, restoration, and facilitate encoding of the image." at column 26, line 22).

**Regarding Claim 16**, Chow discloses the system of claim 15, wherein the GPU is adapted to receive blocks of pixels that an image has been separated into, and process each block of pixels (Referring to Figure 28, numeral 20 (PCI Local Bus), the portion of Figure 28 allows the graphics controller (26) of Figure 2 to show that it is connected to the PCI Local bus), in parallel ("Similarly, the order of operations is important to developing the optimal solution...by allowing IDCT and DCT to be executed in parallel."

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at column 45, line 36), by multiplying a column or row of pixels of an image with a predetermined matrix to generate a corresponding set of output pixels ("Referring now to FIG. 31A, the above described approach to DCT and IDCT computing can be provided via the DCT Unit data path implementation 674, which is shown to include 4 functional units. The fourth unit is a multiplier unit 678." at column 45, line 41); determining sets of scanlines based on the sets of output pixels (Referring to Figure 33, numeral 651(RAM Address Wordline; "Here, the coefficients are stored using the specific ordering and location in structure 720 to support transformation of the 8.times.8 pixel array of FIG. 32." at column 47, line 36); and for each set of scanlines, sampling the pixels comprised within the scanlines and multiplying the sampled pixels with a row or column of the predetermined matrix (Referring to Figure 33, DCT Double Buffer Addressing; Operands 0 and 7 are found stored on address line 0 in diagram 651, with operand 0 on the left half and operand 7 on the right half, the same order as was found for operands 2 and 5." At column 48, line 10).

**Regarding Claim 17**, Chow discloses the system of claim 16, further comprising a central processing unit (CPU) coupled to the GPU by a system bus, the CPU capable of separating the image into the blocks of pixels (Referring now to FIG. 2, a computer system 10 for use with the present invention is shown to include a central processing unit (CPU) 12...Also coupled to the PCI bus is a graphics controller 26..." at column 5, line 44).

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**Regarding Claim 19**, Chow discloses the system of claim 16, wherein the GPU comprises a separate shader for sampling the pixels comprised within each set of the scanlines ("Raw, analog video data are received by the color decoder 33 ...according to the CCIR601 standard at either an NTSC format of 720 pixels x 480 scan lines at 29.97 frames/second, or PAL format of 720 pixels x 576 lines at 25 frames per second." At column 6, line 18).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mia M. Thomas whose telephone number is 571-270-1583. The examiner can normally be reached on Monday-Friday 7:30am-5pm.

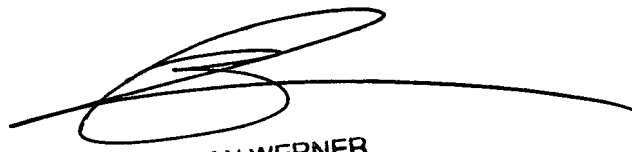
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on 571-272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Mia M Thomas  
Examiner  
Art Unit 2609

*attms*

  
BRIAN WERNER  
SUPERVISORY PATENT EXAMINER